

WHAT IS CLAIMED IS:

1 1. A computer system, comprising:
2 a non-cached multi-ported memory;
3 a central processing unit coupled to the multi-ported
4 memory;
5 a peripheral device coupled to the multi-ported memory;
6 the central processing unit and the peripheral device
7 being configured to access the multi-ported memory
8 independently.

1 2. The system of claim 1, further comprising an
2 operating system executing on the central processing unit,
3 wherein the operating system is configured such that accesses
4 to the multi-ported memory are not cached.

1 3. The system of claim 1, wherein the multi-ported
2 memory is dual-ported.

1 4. The system of claim 1, wherein the multi-ported
2 memory is embedded within a memory controller.

1 5. The system of claim 4, wherein the multi-ported
2 memory and memory controller are integrated into a single
3 chip.

Sub A5
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6. The system of claim 1, wherein the multi-ported memory is static random access memory or dynamic random access memory.

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7. The system of claim 1, wherein the multi-ported memory stores reservation bits mapped to blocks of general-purpose memory in the multi-ported memory.

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8. The system of claim 1, wherein virtual addresses within multi-ported memory are mapped to physical addresses with smart addressing.

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9. The system of claim 1, wherein the coupling of the peripheral device to the memory controller includes an input/output bus.

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10. A method comprising:
making, from a peripheral device, a data access to memory in a computer;
making, from the peripheral device, a status access to memory in the computer;
routing the data access to a first memory in the computer; and

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routing the status access to a second memory in the
computer.

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11. The method of claim 10, wherein the first memory
comprises main memory.

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12. The method of claim 10, wherein the second memory
comprises memory included in a memory controller.

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13. The method of claim 10, wherein the second memory is
dual-ported.

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14. An article comprising a computer-readable medium
which stores computer-executable instructions for memory
accessing, the instructions causing a machine to:

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make, from a peripheral device, a data access to memory
in a computer;

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make, from the peripheral device, a status access to
memory in the computer;

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route the data access to a first memory in the computer;
and

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route the status access to a second memory in the
computer.

Sub C1
1 15. The article of claim 14, wherein the computer
2 includes an input/output controller.

1 16. The article of claim 14, wherein the first memory
2 comprises main memory.

1 17. The article of claim 14, wherein the second memory
2 comprises memory included in a memory controller.

1 18. The product of claim 14, wherein the second memory
2 is dual-ported.

Sub A8
1 19. A method comprising:
2 making, from a central processing unit, a data access to
3 memory in a computer;
4 making, from a peripheral device, a control access to
5 memory in the computer;
6 routing the data access to a first memory in the
7 computer; and
8 routing the control access to a second memory in the
9 computer.

Sub C1
1 20. The method of claim 19, wherein the first memory
2 comprises main memory.

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21. The method of claim 19, wherein the second memory comprises memory included in a memory controller.

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22. The method of claim 19, wherein the second memory is dual-ported.

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23. An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to:

make, from a central processing unit, a data access to memory in a computer;

make, from the central processing unit, a control access to memory in the computer;

route the data access to a first memory in the computer;

and

route the control access to a second memory in the computer.

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24. The article of claim 23, wherein the first memory comprises main memory.

25. The article of claim 23, wherein the second memory comprises memory included in a memory controller.

1 26. The article of claim 23, wherein the second memory
2 is dual-ported.

1 27. An integrated circuit comprising:
2 a memory controller including at least two electrical
3 ports for coupling to communication channels; and
4 multi-ported memory communicatively coupled to each port.

1 28. The integrated circuit of claim 27, wherein the
2 multi-ported memory is dual-ported.

1 29. The integrated circuit of claim 27, wherein the
2 multi-ported memory is static random access memory or dynamic
3 random access memory.

1 30. The integrated circuit of claim 27, wherein the
2 multi-ported memory stores reservation bits mapped to blocks
3 of general-purpose memory in the multi-ported memory.

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